)LQH 3LWFK +LJK %DQG 3DVVEDQG)LOWHU &RQFHQWUDWH 'HY

E\

0LQJ &KH 67$76 &KLS3$& 3WH /WG
6WDQOH\ /LQ 0HGLD7HN ,QF
,DQ +VX 0HGLD7HN ,QF
&KL <XDQ &KHQ 0HGLD7HN ,QF
1DP-X &KR 67$76 &KLS3$& .RUHD /WG

2ULJLQDOO\ SXEOLVKHG LQ 0LFURHOHFWURQLFV 3DFNDJLQJ
:DUVDZ 3RODQG 6HS

&RS\ULJKW ‹

%\ FKRRVLQJ WR YLHZ WKLV GRFXPHQW \RX DJUHH WR DOO
FRS\ULJKW ODZV SURWHFWLQJ LW

solve the constraints of larger die and/or package size limitations, top memory with wide I/O counts as well as customized mobile memory applications [6]. Moreover, since emerging markets are driving advanced technologies in high performance mobile devices, assembly cost is still the major issue to be addressed. As the substrate cost is always the significant factor in a flip chip package, flip chip assembly with a low cost substrate has become a hot topic in the industry. The flip chip interconnect with Cu pillar bond-on-lead (BOL) structure on embedded trace substrate (ETS) has been widely adopted for low cost demand. The flip chip interconnect with Cu pillar BOL and enhanced processes (fcCuBE®) can also help to deliver a high performance packaging solution with a cost effective mass reflow (MR) manufacturing process [7]. Therefore, in order to develop the technology of a fine pitch high bandwidth fcPoP, a test vehicle of package size around 200mm^2 with a top interposer substrate that interconnects the top mobile memory and bottom package peripherally by using Cu posts was evaluated in this paper, which the schematic is shown in Fig. 1. Different top and bottom ball pitch to connect top mobile memory and bottom packages can be designed in this utilized top interposer substrate. The fine Cu post pitch of 0.23mm on an interposer (connects to bottom substrate) and solder ball pitch of 0.35mm on the bottom substrate (connecting to printed circuit board) was utilized. With this high bandwidth fcPoP structure, die size limitations can be overcome by using this finer interconnection pitch, providing the flexibility to allow any memory interface pitch application. Furthermore, through this developed result, it not only illustrated this package can meet warpage and coplanarity targets but also can pass the long term package reliability conditions without any failure observed. It shows that this high bandwidth fcPoP architecture is an enabling technology for highly integrated, miniaturized, low profile and cost-effective 3D packaging solutions.

Fig. 1. Schematic of a high bandwidth fcPoP

II. CHARACTERIZATION OF HIGH BADNWIDTH FCPOP

As the fcPoP stacks fully tested memory and logic packages to eliminate known good die (KGD) issues, it provides flexibility in mixing and matching IC technologies and enables assembly of larger dies in a thinner PoP stack up with finer top ball pitch. The fcPoP is typically adopted as the ideal solution with its overmold configuration that provides better warpage performance and drives aggressive package height reductions and finer mobile memory pitch down to 0.4mm and below. The surface treatment of CuOSP on the bottom substrate and top memory interface pads is typically utilized and can support down to 0.3mm minimum ball pitch on bottom/BGA pads and much finer pitch on top memory interface pads of the bottom package. Both capillary underfill (CUF) and molded underfill (MUF) are available in fcPoP, although MUF technology allows for increased cavity size and larger die size with a lower assembly cost solution. However, the continued demands for higher level integration has led the industry to evaluate new fcPoP technologies to be utilized with stacking of wide I/O counts and/or next generation mobile memory. The high bandwidth fcPoP technology is one of the new technology solutions to achieve these goals, featuring a top interposer substrate that interconnects the top mobile memory and bottom package peripherally by using Cu post, Cu cored solder ball (CCSB) [8, 9], solder ball [10], etc. In order to develop the technology of high bandwidth fcPoP with Cu post architecture, a test vehicle with package size of ~200mm^2 was utilized. The die size of 75mm^2 and die thickness of 65µm as well as minimum 80µm Cu pillar bump pitch was evaluated. A two-layer (2L) cored substrate with total thickness of 0.11mm was used as top interposer. The Cu posts with 0.23mm pitch, 0.15mm height and 0.12mm diameter were manufactured in this interposer. Thin package profile high bandwidth fcPoP is an important topic in the industry as it added a top interposer subst [10 al p [1-8 0 -1.157 T01.7(

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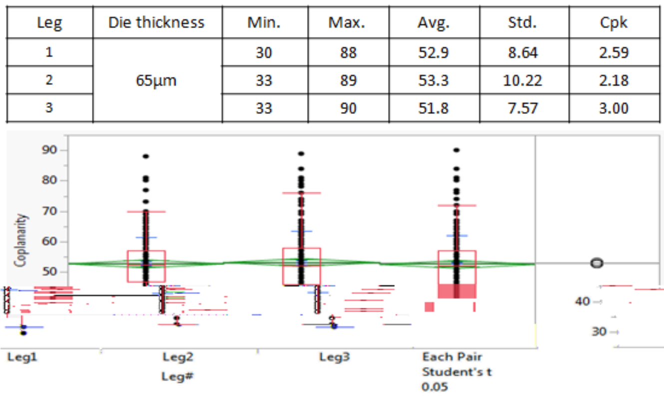
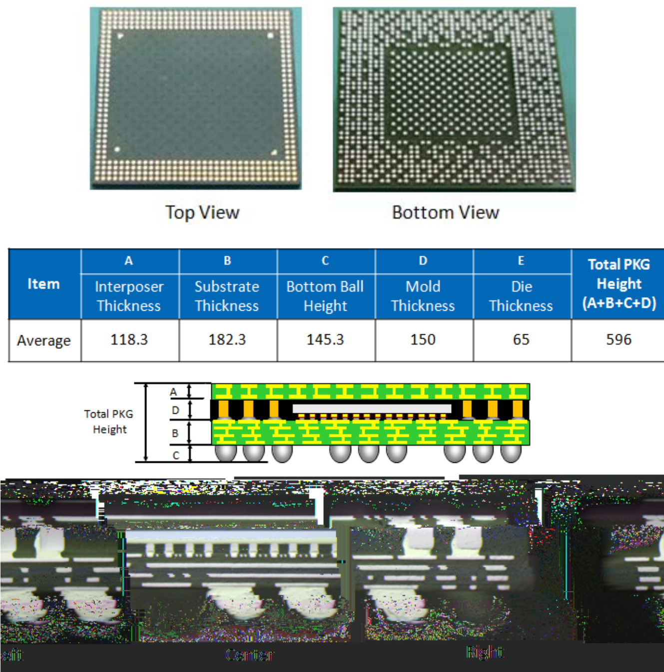
bandwidth fcPoP, it can reduce the non-wet risk in Surface Mount Technology (SMT) processes and guarantee the good yield performance after SMT. In addition, through the coplanarity assessment illustrated in Fig. 8, it was found that all three legs shows good coplanarity less than 90µm and good Cpk values greater than 2.0. It also indicates that the process is consistently under control with higer Cpk value. For the purpose of measuring total package height, the cross-sectional image of this high bandwidth fcPoP was illustrated in Fig. 9, which indicates the average package height is around 596µm (without stacking top memory). Moreover, through the cross sectional inspection, it also showed the good Cu pillar bump and Cu post interconnection joints after assembly processes.



Leg	Die thickness	Min.	Max.	Avg.	Std.	Cpk
1	65µm	30	88	52.9	8.64	2.59
2		33	89	53.3	10.22	2.18
3		33	90	51.8	7.57	3.00

Fig. 8. Coplanarity behaviors in a high bandwidth fcPoP with 4L ETS



Item	A Interposer Thickness	B Substrate Thickness	C Bottom Ball Height	D Mold Thickness	E Die Thickness	Total PKG Height (A+B+C+D)
Average	118.3	182.3	145.3	150	65	596

Fig. 9. Cross-sectional view in high bandwidth fcPoP

III. LONG-TERM RELIABILITY TEST ASSESSMENT

In order to validate the package reliability of this high bandwidth fcPoP with 4L ETS, this package was evaluated in long term reliability tests such as pre-condition of moisture sensitivity level (MSL3A) as well as unbiased highly accelerated stress test (uHAST) of 96 hours (with pre-condition of MSL3A) and extended to 192 hours, thermal cycling test condition B (TCB) of 1000 cycles (with pre-condition of MSL3A) and high temperature storage test (HTST) of 1000 hours. The long-term package reliability results and images of all three legs based on utilizing Through Scanning Acoustic Microscopy (T-SAM) inspection after uHAST 192 hours, TCB 1000 cycles and HTST 1000 hours are illustrated in Fig. 10. From Fig. 10, it is observed that there is no abnormality observed through T-SAM images. In order to realize the solderability of Cu post interconnections that connect to bottom substrate, the cross-sectional images after uHAST 192 hours, TCB 1000 cycles and HTST 1000 hours that utilized Scanning Electro Microscopy (SEM) technology were shown in Fig. 11. From Fig. 11, it is clearly indicated that there is no solder bridge as well as non-wet phenomena found after the long-term reliability test. Based on these reliability test result, it not only shows that the illustrated 4L ETS high bandwidth fcPoP examined in this study can guarantee low package profile assembly without any yield loss and solder bridge, but also meet the reliability criterion. Therefore, it is believed that with the technology established in this paper for high bandwidth fcPoP can provide a highly integrated, miniaturized and low profile 3D packaging solution in semiconductor industry.

Leg#	Die Thickness	Reliability Test Results						
		MSL3A	MSL3				HTST 500hrs	HTST 1000hrs
			uHAST 96hrs	uHAST 192hrs	TCB 500x	TCB 1000x		
1	65um	0/45	0/45	0/45	0/45	0/45	0/45	0/45
2		0/45	0/45	0/45	0/45	0/45	0/45	0/45
3		0/45	0/45	0/45	0/45	0/45	0/45	0/45

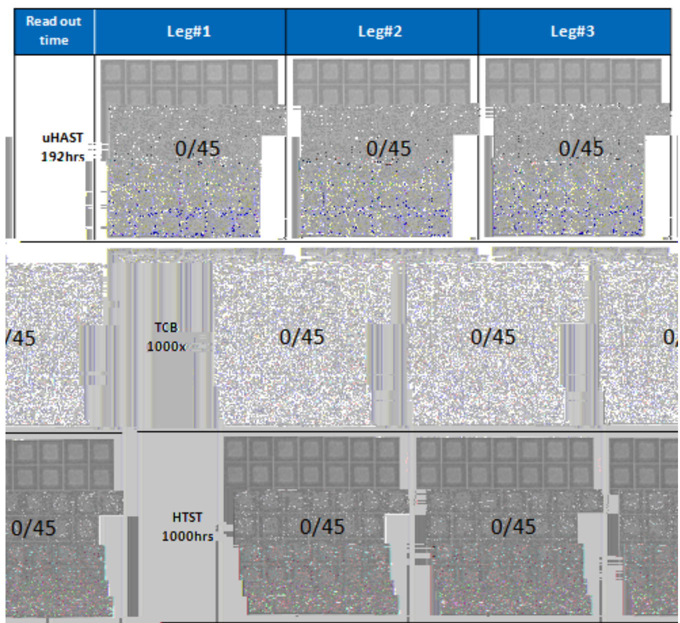
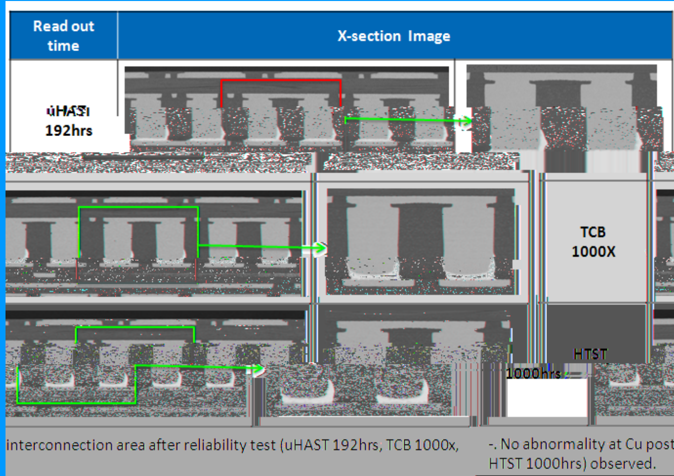


Fig. 10. Long term package reliability result and T-SAM image inspection in a 4L ETS high bandwidth fcPoP



interconnection area after reliability test (uHAST 192hrs, TCB 1000x, HTST 1000hrs) observed.

-. No abnormality at Cu post